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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/623,655	09/07/2000	Takafumi Maruyama	43889-977	6288

7590 06/29/2004

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/623,655	MARUYAMA ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 13th of May 2004. Claims 1, 2 and 13 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 15th of January 2004. Currently, claims 1, 2, 4-9, 13 and 14 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 1 recites the broad recitation "said bus selector device selecting among connection of said plurality of buses in accordance with the connection information" in lines 6-7, and the claim also recites "said bus selecting among connections of the plurality

of buses in accordance with the switch signal" in lines 12-13, which is the narrower statement of the range/limitation.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1, 2, 4-8, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata [JP 404133154 A; cited by the Applicants] in view of Shibazaki [US 5,809,257 A] and what was well known in the art, as exemplified by Kawagoe [US 6,208,548 B1].

Referring to claim 1, Murata discloses a semiconductor integrated circuit system (i.e., bus switching control system in Fig. 1) having a plurality of units (i.e., bus masters 1a-c and slaves 4a-c in Fig. 1) and making said plurality of units transmit and receive signals to and from each other (See page 362+, the left, lower paragraph [operation]), comprising: a bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1) connected to said plurality of units via a plurality of buses (i.e., bus 10a and bus 10c in Fig. 1), said bus selector device receiving connection information among said plurality of units (i.e., receiving access information, viz., REQ signal and address data in Fig. 2) and selecting among connections of said plurality of buses in accordance with said connection information (See page 363+, the left, upper paragraph [embodiment]), wherein said bus selector device (i.e., bus switching circuits and bus selecting circuits) is further provided with a second latch circuit (i.e., FF 26-28 in Fig. 4) in which a switch signal (i.e., decoded address signal from address decoder 14 and gate enable signals within FF 26-28 in Figs. 3 and 4) is held (i.e., gate enable signals are latched in f/fs), said bus selector device outputs said switch signal in accordance with said connection information among said plurality of units (See page 363, the right, lower paragraph, lines 6-11) and selects among connections of said plurality of buses in accordance with said switch signal (See page 363+, the left, upper paragraph [embodiment]).

Murata does not expressly teach said bus selector device being provided with latch means for holding signals to be transmitted to or received from said plurality of units to adjust timings of signal transmission and reception.

Shibazaki discloses a bus control apparatus for data transfer system (Fig. 7), wherein a bus selector device (i.e., data selector 22 and 23 in Fig. 8) being provided with latch means for holding (i.e., buffer section 20, 25 and data holding section 21, 24 in Fig. 8) signals to be transmitted to or received from a plurality of units (i.e., memories, e.g., MEMORY A and B in Fig. 8) to adjust timings of signal transmission and reception (See col. 7, lines 51-59 and Fig. 9A-F).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said latch means for holding signals (i.e., buffer section and data holding section), as disclosed by Shibazaki, in said bus selector device, as disclosed by Murata, for the advantage of improving the reliability and operability of said semiconductor integrated circuit system (See Shibazaki, col. 4, lines 35-37).

Murata, as modified by Shibazaki, does not expressly teach said plurality of units are a plurality of chips.

The Examiner takes Official Notice that said plurality of units are a plurality of chips, such as memory chips, is well known to one of ordinary skill in the art of memory architecture, as evidenced by Kawagoe (See Fig. 1 and col. 4, lines 53+ [Embodiment 1]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized said plurality of units (i.e., bus masters and slaves), as disclosed by Murata, as a plurality of chips (i.e., memory chips), as disclosed by Kawagoe, since it would have the same structure of master-slave relationship among devices for bus communicating application (e.g., memory read/write operations).

Referring to claim 2, Murata teaches said bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1) comprising switch means for switching (i.e., gates 11-13 in

Fig. 3 and gates 15-17 in Fig. 4) among said connections of said plurality of buses (See Fig. 1) in accordance with said switch signal (i.e., gate enable signal open the gate 15-17 for the selected bus connection in Fig. 4); and determination means for determining (i.e., address decoder 14 of Fig. 3 and gates G20-G22, FF 26-28 in Fig. 4) said connection information among said plurality of chips received (i.e., received access information, viz., REQ signal and address data in Fig. 2), and for outputting said switch signal (i.e., gate enable signals in Figs. 3 and 4) in accordance with determination results to said switch means (See page 363, the left, upper paragraph, lines 14-18).

Referring to claim 4, Murata teaches said plurality of chips (i.e., bus masters 1a-c and slaves 4a-c in Fig. 1) include at least one master chip (i.e., bus masters 1a-c in Fig. 1) and a plurality of slave chips (i.e., slaves 4a-c in Fig. 1).

Referring to claim 5, Murata teaches said master chip (e.g., bus master 1a of Fig. 1) outputs said connection information among said plurality of chips (i.e., access information, viz., REQ signal and address data in Fig. 2) to said bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1); and said master chip and said bus selector device are connected to each other (See Fig. 2) with a single bus (i.e., bus 10a-1 of Fig. 2), said single bus carrying said connection information among said plurality of chips (See page 363, the left, upper paragraph, line 19 through the right, lower paragraph, line 1).

Referring to claim 6, Murata teaches said master chip (e.g., bus master 1a of Fig. 1) outputs said connection information among said plurality of chips (i.e., access information, viz., REQ signal and address data in Fig. 2) to said bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1); and said master chip and said bus selector device are connected to each other (See Fig. 2) with two or more buses (See page 363, the left, upper paragraph, lines 12-14; i.e., wherein in fact that the bus 10a-1, 10b-1-1 ~ 10b-1-3 are consisted of a plurality of signal lines for address, data, control signal, etc., impliedly suggests that the bus, e.g., bus 10a-1 of Fig. 2, comprises two or more

buses, such that address bus, data bus, control signal bus, etc.), one of said two or more buses (i.e., address bus and control signal bus) carrying said connection information among said plurality of chips (i.e., access information).

Referring to claim 7, Murata teaches said two or more buses the bus (e.g., bus 10a-1 of Fig. 2 comprises two or more buses, such that address bus, data bus, control signal bus, etc.) include a command bus (i.e., address bus and control signal bus for REQ signal), said command bus being also used as a connection information bus to carry said connection information among said plurality of chips (i.e., as a bus for transferring access information, viz., REQ signal and address data; See Fig. 2).

Referring to claim 8, Murata teaches said one of said two or more buses (i.e., address bus and control signal bus for REQ signal) to carry said connection information among said plurality of chips (i.e., access information, viz., REQ signal and address data in Fig. 2) is a specifically designed connection information bus (i.e., specifically designed bus carrying address and control signal for REQ signal).

Referring to claim 13, Murata discloses a bus selector device (i.e., bus switching circuits 2a-c, bus selecting circuits 3a-c and bus 10b in Fig. 1) connected to a plurality of units (i.e., bus masters 1a-c and slaves 4a-c in Fig. 1) with a plurality of buses (i.e., bus 10a and bus 10c in Fig. 1) and selecting among connections of said plurality of buses (See page 363+, the left, upper paragraph [embodiment]), comprising: switch means for switching (i.e., gates 11-13 in Fig. 3 and gates 15-17 in Fig. 4) among said connections of said plurality of buses (See Fig. 1) in accordance with a switch signal (i.e., gate enable signal open the gate 15-17 for the selected bus connection in Fig. 4); determination means for receiving and determining (i.e., address decoder 14 of Fig. 3 and gates G20-G22, FF 26-28 in Fig. 4) connection information among said plurality of units (i.e., access information, viz., REQ signal and address data in Fig. 2), and for outputting said switch signal (i.e., gate enable signals in Figs. 3 and 4) in accordance with determination results to said switch means (See page 363, the left, upper paragraph, lines 14-18); data input means for receiving data (e.g., means for receiving data through data signal lines within bus 10a-1

in Fig. 1) from any one of said plurality of units (i.e., bus master 1a of Fig. 1); data output means for outputting said data (e.g., means for outputting said data through data signal lines within bus 10c-1 in Fig. 1) to at least one of said plurality of units (i.e., slave 4a of Fig. 1) via one of said plurality of buses (i.e., bus 10a-1 and bus 10c-1 in Fig. 1) that is selected by switching of said switch means (i.e., selected by gates 11 in Fig. 3 and gate 15 in Fig. 4); and internal buses (i.e., bus 10b in Fig. 1) connected to said plurality of buses (i.e., bus 10a and bus 10c in Fig. 1); and a plurality of latch circuits (i.e., FF 26-28 in Fig. 4) hold said switch signal (i.e., gate enable signals are latched in f/fs).

Murata does not teach a plurality of latch circuits arranged on said plurality of internal buses.

Shibazaki discloses a bus control apparatus for data transfer system (Fig. 7), wherein a plurality of latch means (i.e., buffer section 20, 25 and data holding section 21, 24 in Fig. 8) arranged on a plurality of internal buses (i.e., bus lines 200 and signal lines 201 and 202 in Fig. 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said latch means for holding signals (i.e., buffer section and data holding section), as disclosed by Shibazaki, in said bus selector device, as disclosed by Murata, so as to adjust timings of signal transmission and reception (See Shibazaki, col. 7, lines 51-59 and Fig. 9A-F) for the advantage of improving the reliability and operability of said semiconductor integrated circuit system (See Shibazaki, col. 4, lines 35-37).

Murata, as modified by Shibazaki, does not expressly teach said plurality of units are a plurality of chips. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized said plurality of units (i.e., bus masters and slaves) as a plurality of chips (i.e., memory chips), which has been discussed / addressed above in the claim 1.

Referring to claim 14, Murata teaches control signal input means for receiving a control signal (e.g., means for receiving control signal through control signal lines within bus 10a-1 in Fig. 1) from one of said plurality of chips (i.e., bus master 1a of Fig. 1) for another chip (i.e., slave 4a-c in Fig. 1); and

control signal output means for outputting said control signal (e.g., means for outputting said control signal through control signal lines within bus 10c-1 in Fig. 1) to at least one of said plurality of chips (i.e., slave 4a of Fig. 1) through one of said plurality of buses (i.e., bus 10a-1 and bus 10c-1 in Fig. 1) selected by switching of said switch means (i.e., selected by gates 11 in Fig. 3 and gate 15 in Fig. 4).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata [JP 404133154 A] in view of Shibazaki [US 5,809,257 A] as applied to claims 1, 2, 4-8, 13 and 14 above, and further in view of Gates et al. [US 5,920,708 A; hereinafter Gates].

Referring to claim 9, Murata, as modified by Shibazaki, discloses all the limitations of the claim 9 except that does not teach said connection information among said plurality of chips is composed of a packet.

Gates discloses a single pin serial port for information transfer (See Abstract and Fig. 3), wherein connection information (i.e., command byte 410 of Fig. 4B; See col. 9, lines 18-27) among a plurality of chips (i.e., LED 350, Soft Resource 360, Programmable Logic Circuit 330, Board Control Logic 370, SEEPROM 380, EEPROM 390 and Bus Terminators 360 in Fig. 3) is composed of a packet (i.e., command packet 420 of Fig. 4B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said feature of single pin serial port with support circuit, as disclosed by Gates, in said bus selector device, as disclosed by Murata, as modified by Shibazaki, so as to communicate in a serial communication mode among said plurality of chips, for the advantage of less pins on said plurality of chips (i.e., two interconnected integrated circuits), less PCB etch routing, reduced timing constraints of multi-signal interface (viz., parallel bus interface) by elimination of signal-to-signal skew concerns (See Gates, col. 7, lines 8-13).

Response to Arguments

7. Applicant's arguments with respect to claims 1, 2, 4-8, 13 and 14 have been considered but are moot in view of the new ground(s) of rejection. In contrary to the Applicants' allegation, Murata in the prior art of record suggests the newly claimed limitation "a latch circuit in which a switch signal is held". Moreover, in response to the Applicants' argument that the Examiner's conclusion of obviousness for the *35 USC §103(a)* rejection fails to establish a *prima facie* case of obviousness, the Examiner respectfully disagrees. In contrary to the Applicants' statement, all the rejections under *35 USC §103(a)* in the prior and the instant Office Action established a *prima facie* case of obviousness meeting the three basic criteria of the MPEP 2143.03 (8th ed. 2001). See the prior and instant Office Actions. And, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner has clearly pointed out rationale for appropriate combination of the references. Thus, the Applicants' argument on this point is not persuasive.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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